FAIRCHILD

FAN-OUT

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Editor—W. O. Hamlin

10-MC EPITAXIAL INTEGRATED FUNCTIONAL BLOCKS

- NINE FUNCTIONAL ELEMENTS
- 15 OHMS COLLECTOR SATURATION RESISTANCE
- 10-MC CIRCUIT OPERATION
- RELIABILITY SPECIFICATION

Fairchild silicon planar epitaxial Micrologic integrated microcircuits, successors to non-epitaxial Micrologic,* are functional blocks composed of 25-mc NOR gates, requiring 15 mW per node. The new devices increase speed, noise margin, and separation of logic levels throughout the temperature range. Shown in Fig. 1 is the basic NOR gate schematic, profile of construction, and the 8-leaded TO-5-style package of Micrologic. (TO-47-style cans are also available.)

The data sheet specifies minimum and maximum limits on electrical functional parameters which guarantee fan-in and fan-out for all conditions of "worst case" design. The worst case design used assures that fan-in and fan-out rules are valid even after all individual transistor and resistor component tolerances simultaneously reach 1000-hour burn-in test limits in all specified logic interconnections. The worst case design includes: (1) transistor and resistor component tolerances; (2) logic arrangements or interconnections; (3) power supply variations.

The new construction includes a 450-ohm resistor in series with each transistor base resulting in a 300% improvement in noise immunity and current hogging. In addition, the planar epitaxial process allows a number of improvements: Lower collector saturation resistance, particularly at the critical +125°C temperature, smaller transistor geometry, and lower parasitic capacitances due to closer spacing between elements. As a result, epitaxial Micrologic has the following characteristics which are most important to circuit design:

1. Noise margin typically 310 mV at 25°C in worst-case circuit.
2. 50 ns minimum pulse width for reliable triggering.

* *Non-epitaxial Micrologic has been in use for several years in logic systems and for ground, airborne, and space installations.*

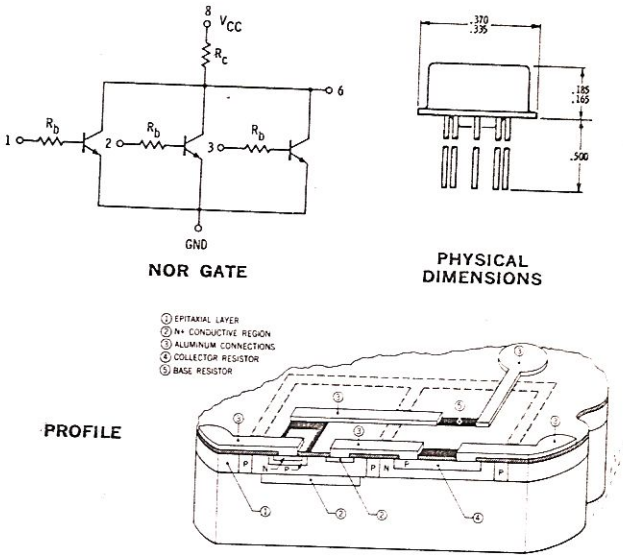


Fig. 1. Micrologic integrated circuit.

3. 11 ns typical t_{pd} at 15 mW per node (basic gate).

The following guarantees of reliable operation over the full military temperature range are provided:

1. Electrical limits at −55°C to +125°C are guaranteed. (See Note below.)
2. Fairchild Assured Customer Test Program (FACT), which can be included as part of the purchase contract, contains guaranteed limits for operating life provided by testing on a sample basis after a 1,000-hour burn-in.

NOTE: For ground-support equipment or systems operating in a controlled environment, elements at lower prices are also available which meet all the electrical requirements except that the temperature extremes are 0-75°C.

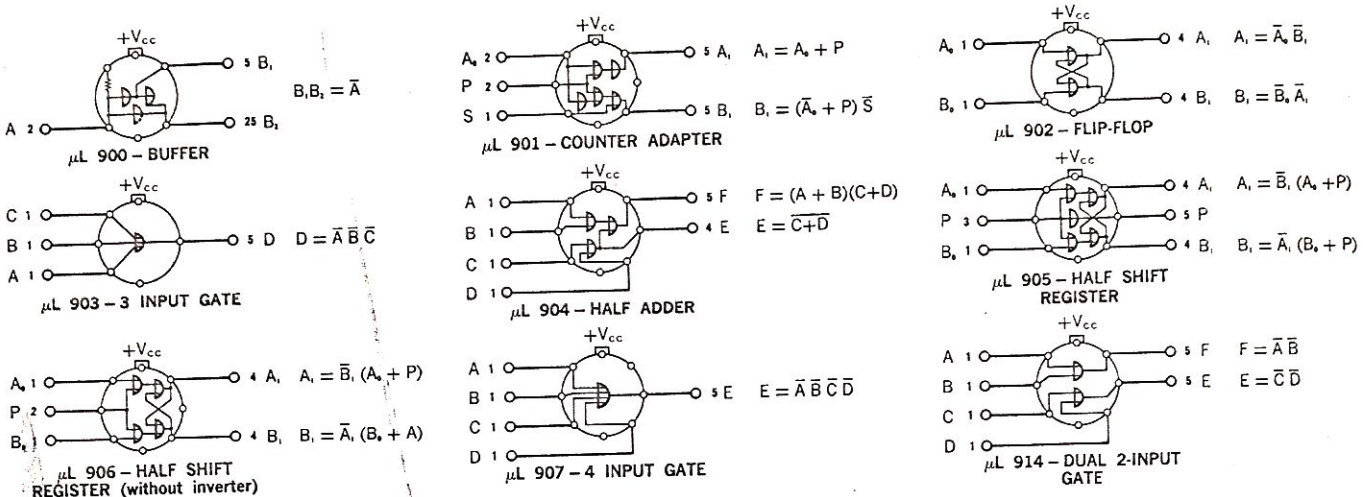


Fig. 2. Logic diagram, equations, and loading characteristics for the 9 Micrologic elements.

NINE ELEMENTS AVAILABLE

The Micrologic line consists of 9 elements which may be combined in various ways for lowest cost, minimum number of cans, or both, to meet any particular requirement (see Fig. 2). These elements include three which were not in the previous non-epitaxial catalog: Compared with the corresponding original elements, the newer units offer a reduction of elements of up to 50% for many applications. In addition, recent price reductions make them more attractive from the viewpoint of economy. The additional elements are as follows:

1. The 4-input gate reduces requirements by one can when a *fan-in* of 4 is required.
2. The dual 2-input gate is more economical for inverters, non-inverting 2-input gates, and flip-flops.
3. The half-shift-register element without inverter, used for the second rank of a double-rank storage register, costs less than its counterpart with inverter, needs less drive to pin 2 (equal to 1 load), and dissipates 21 mW less power in the worst case at 25°C.

Figure 3 shows a possible combination of the 2-input dual gate and the 4-input gate compared with the same logic using the 3-input gate only.

THE MICROLOGIC DATA SHEETS

Complete test data, ratings, characteristic curves, and descriptions of the 9 elements are contained in an 18-page data sheet. With the aid of this document and the Fairchild Microcircuits Handbook, the logic circuit engineer can design reliable logic systems for military or commercial applications.

D-c Tests and Limits. The basic NOR gate can serve as an example of margins provided by the tests for high and low signal levels. Figure 4 shows these typical levels versus fan-out and temperature with shaded marginal areas. As the elements are compatible, one table of limits on page 2 of the data

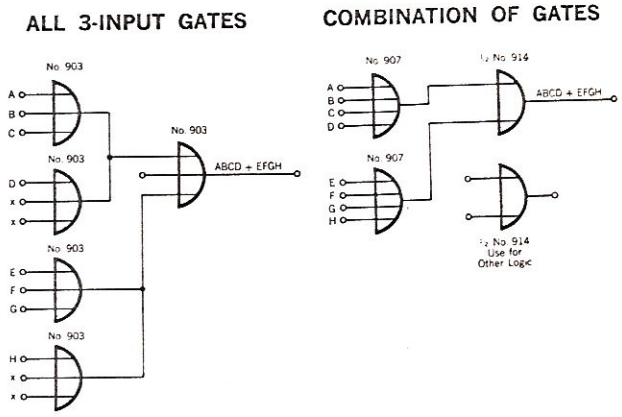


Fig. 3. Economy of circuitry using the 4-input gate and 2-input dual gate in comparison with all 3-input gates.

sheet serves for all. These limits correlate with the list of tests given with the data for each element. The conditions and limits are shown symbolically with numerical tolerances. V_{HIGH} and V_{LOW} are general terms used here rather than the data sheet symbols for a particular test. The several test conditions to be met are as follows:

1. When V_{HIGH} minimum is applied to any or all inputs, the output must be below V_{LOW} maximum.
2. When V_{LOW} maximum is applied to any or all inputs, the output must be above V_{HIGH} minimum. The worst possible d-c case occurs when V_{LOW} maximum is simultaneously applied to all inputs. A further condition tested for and guaranteed is minimum current flow (I_A minimum) from the output pin at −55°C, 25°C and +125°C.
3. With V_{HIGH} applied to any input (and parallel inputs worst-cased by clamping), I_{IN} is $\leq I_A$/Fan-Out.

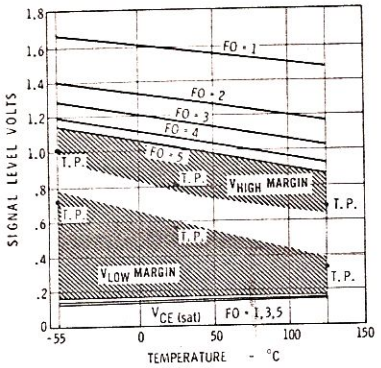


Fig. 4. Typical signal levels versus fan-out and temperature.

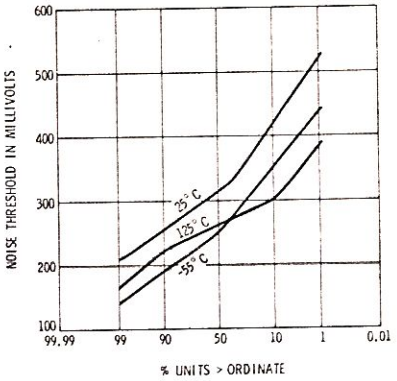


Fig. 5. Cumulative distribution of noise threshold.

Noise Immunity Curves and Measurements.* Micrologic noise immunity is evaluated by measuring in the ground lead (the most sensitive point) the Noise Threshold Signal necessary to interrupt the logic state. Measurements at −55°C, 25°C and 125°C are performed in a worst-case circuit — fan-out of 5, worst possible current hogging, and a simulated infinite chain of gates. A random sample of elements is used in each test of the Noise Threshold Signal.

Results of testing a large number of gate samples, shown in Fig. 5, confirm the V_{SIGNAL} curve of Fig. 4. In 99% of the tests run, D-C Noise Threshold is above 150 mV at the worst temperature of −55°C. It should be emphasized that this figure is derived from the worst-case circuit, which will seldom be encountered in normal logic. Furthermore, regular gating arrangements, shifting, counting, etc., seldom use a fan-out of 5. Elements other than gates exhibit even higher d-c noise immunity, particularly those with internal nodes.

Figure 5 gives the distribution of noise immunity at 25°C and temperature extremes. Not shown but available are curves showing that noise immunity is essentially constant with V_{cc} variations of ±20% at +125°C. Noise threshold improves as V_{cc} increases above 3.0 volts at −55°C. Noise threshold drops off only 50 mV as V_{cc} is reduced to 2.4 volts at −55°C, or well beyond normal V_{cc} supply range. This further indicates −55°C margins can be substantially enhanced if provisions are made to increase V_{cc} at the colder temperatures.

Pulse Noise Threshold is greater than the d-c threshold. For square-wave pulses of less than 50 ns, it is 300 mV (2 x 150 mV d-c) in 99% of the measured samples at all temperatures (see Fig. 6).

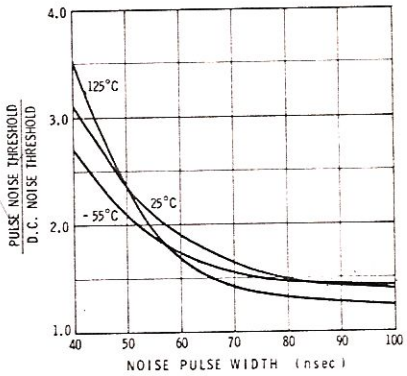


Fig. 6. Pulse noise immunity versus noise pulse width.

Delay Time Characterized. Minimum and maximum switching times at 25°C and switching delay times versus temperature are typically characterized in the data sheet for different input and output loading.

The switching delays of the integrated circuits vary according to the complexity of the element, the number of external loads and temperature. For any condition of temperature and load for the gate using a positive pulse input, delay time is typically from 9 ns to 22 ns. Reliable switching of the storage elements (Part Nos. 902, 905 and 906) is conservatively stated as 50 ns minimum pulse width, and there are no transient conditions in this direct coupled NOR circuitry to contend with (no turn-off bias or speed-up capacitors). The major cause of timing mismatch comes from storage time of saturated transistors, which is worst-case at +125°C. Figure 7, an oscillogram of a No. 905 element counting at 10 mc, 25°C, shows that there is no degradation between input and output waveforms; that rise time is about 15 ns; and that fall time is about 10 ns.

* *Detailed analysis of noise immunity is covered in APP-89, to be published.*

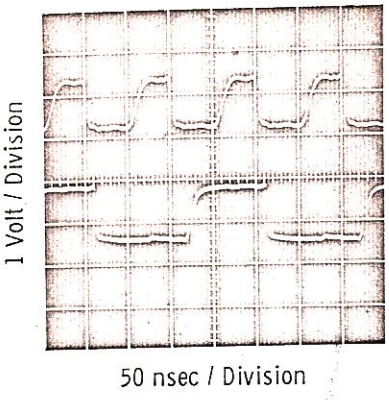


Fig. 7. Wave forms of binary stage counting at 10 mc, 25°C.

Fact Program. FACT stands for "Fairchild Assured Customer Test." The FACT section of the data sheet is a complete procurement specification which can be referred to as a purchase contract. It covers detailed requirements for highly reliable Planar Epitaxial Micrologic devices suitable for extreme environment applications such as use in space vehicles. The FACT specification provides quality assurance at minimal cost to the buyer since the required series of tests and evaluations fit into the in-house routine. It includes tests complying with Military Standard 750, which the customer might otherwise desire on an individual basis at a cost which would be uneconomical to any but buyers of the largest quantities.

The FACT document details acceptance conditions for operation life, storage life and resistance to environmental stress which are obtained by actual test. The specifications include the following parts:

1. Group A Inspection (Electrical Tests).
2. 100% Processing (Environmental Tests).
3. Group B Inspection (Environmental Tests).

Details of Micrologic reliability and test procedures are given in the Micrologic Reliability Report.*

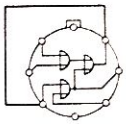
APPLICATIONS

Virtually any logic function can be efficiently mechanized with Micrologic. The 9 elements are not limited to the standard configurations (see Fairchild Microcircuits Handbook for descriptions of basic circuits such as pulse generators, shift registers, and binary counters), but, being compatible, can be connected in an unlimited number of combinations.

Write to Fairchild, Marketing Services Dept., 545 Whisman Road, Mountain View, California.

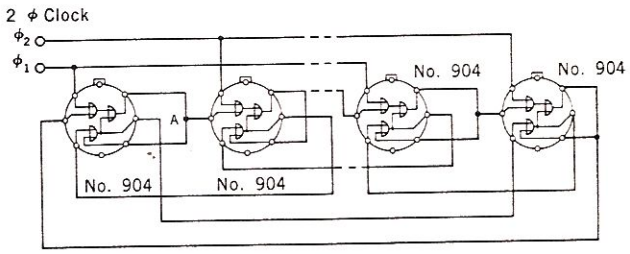
To illustrate the versatility of these elements, a few circuits that can be formed with Micrologic are described below.

1. Half-Gated Flip-Flop. The half adder (Part No. 904) is one of the most versatile Micrologic elements. As shown in the figure, adding one external connection converts it to a flip-flop with one gated input. This circuit can be employed to form ring counters or commutators — with the advantage that it uses fewer components than individual flip-flops and gates.



No. 1

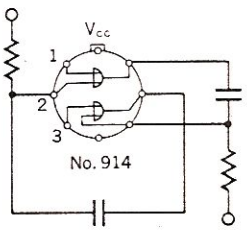
2. Ring Counter. In the design of sequential logic a trade-off can be made between the number of storage elements and size of the output matrix required for a particular number of discrete outputs. Thus the circuit may consist of few storage elements with a large output matrix or more storage elements with a smaller output matrix, up to the point where there is a storage element for each output and no matrix whatever. For example, if 64 outputs are required, the limiting cases can be 12 half shift register elements (Part No. 905) with 64 six-input gates for the matrix, and, at the other extreme, 64 half adder elements (Part No. 904) with no matrix. The latter case would be the ring counter shown in the diagram. As in all ring counters, a means must be provided for assuring a single *one* in the counter initially.



No. 2

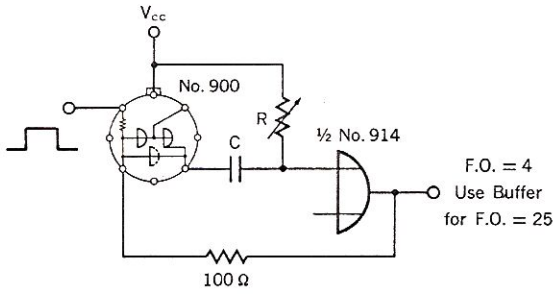
3. Multivibrators.

A. A dual 2-input gate (Part No. 914) can be made into an astable multivibrator by adding capacitive feedback and base bias resistors as shown. The oscillation can be gated by clamping either of the inputs, pin 1 or 3. Speed is limited by the collector resistance through which C is charged.



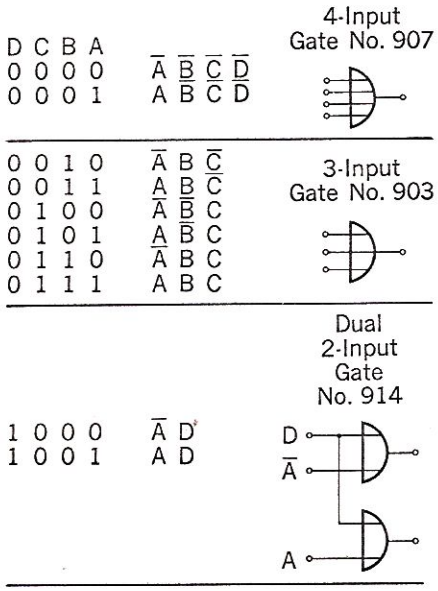
No. 3A

B. A monostable multivibrator can be made with a variation of Circuit A above. Capacitive coupling is used in one feedback loop and direct coupling in the other. As recovery time (charge time of capacitor) is limited by the collector resistance of the gate element, use of the buffer, which has a low-resistance emitter-follower output, for the input stage increases the maximum speed. Use of the buffer in the output stage as well gives more driving power.



No. 3B

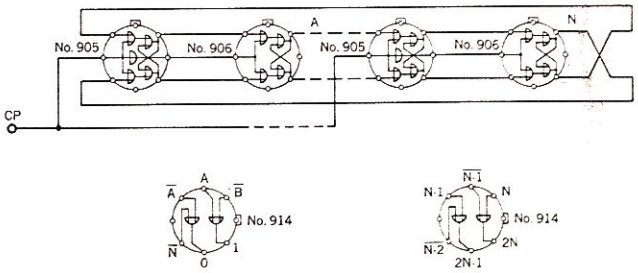
4. Decoding Matrix with Efficient Use of Available Gates. The availability of gates with 2, 3, and 4 inputs makes it possible to construct a decoding matrix with the fewest gates. The count sequence for a 1-2-4-8 decimal counter is illustrated below. Using a 4-input and dual 2-input gates as well as 3-input gates, only 9 Micrologic elements are required. Using only 3-input gates, 12 elements would be required.



No. 4

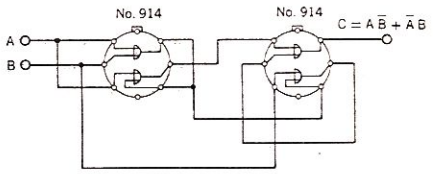
5. Micrologic Shift Counter. A shift register can be used as a counter by connecting the output to the input with a crossover. For moduli of 15 or less this form of counter with decoding matrix can be shown to cost less than binary counters with decoding. It also has the advantage of higher speed as each stage changes at 1/N times the input rate, whereas in a binary counter the least significant stage must operate at the full input rate. (Full details are given in APP85.)

Since the shift counter has a modulus of 2N rather than 2^N, as is characteristic of binary counters, more storage elements are required for a given modulus. The simplicity of output decoding, however, more than offsets this increase.



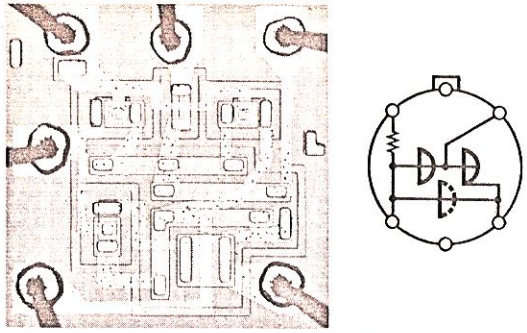
No. 5.

6. Exclusive OR Circuit. An exclusive OR circuit can be composed of two 2-input gates (Part No. 914). This circuit has the advantage that the complements of A and B are not needed. Using the half-adder element (Part No. 904) for this function requires the complements.



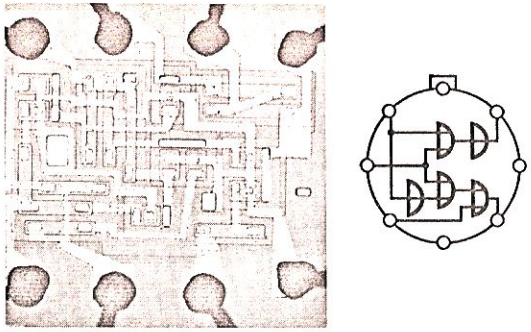
No. 6

SILICON PLANAR EPITAXIAL MICROLOGIC FAMILY



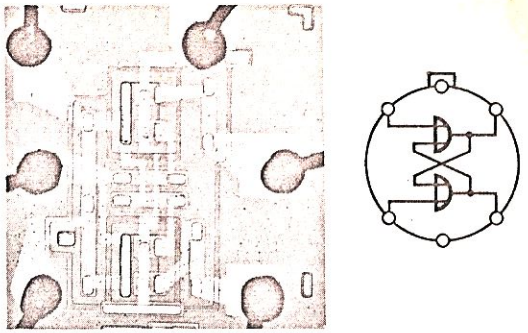
900 BUFFER

A low impedance inverting driver circuit.



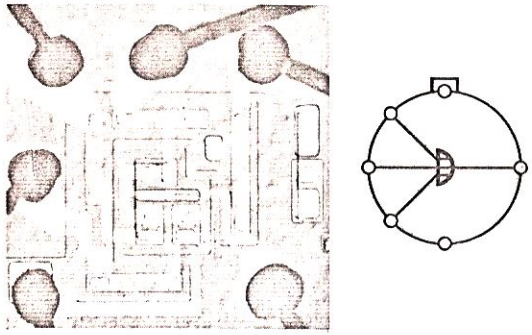
901 COUNTER ADAPTER

Provides gated, non-inverted complementary outputs from a single-valued input.



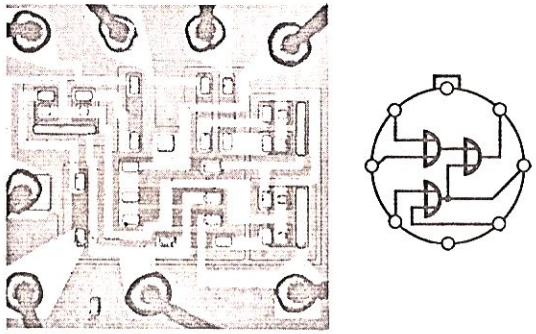
902 FLIP-FLOP

A bistable flip-flop storage unit.



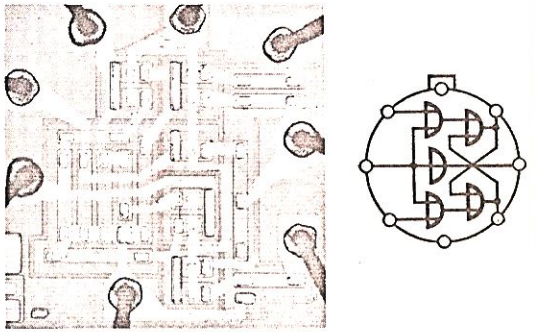
903 THREE-INPUT GATE

A three-input NAND/NOR circuit.



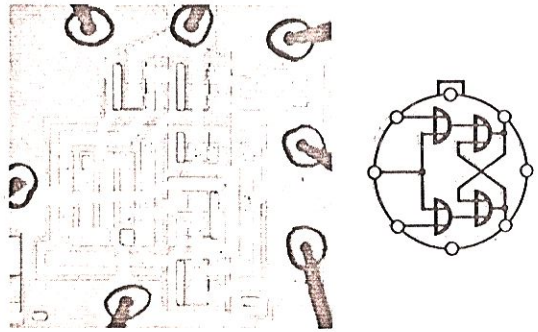
904 HALF ADDER

A two-level AND/OR gate suited for use as a complete half-adder, an exclusive OR gate or any similar logic function.



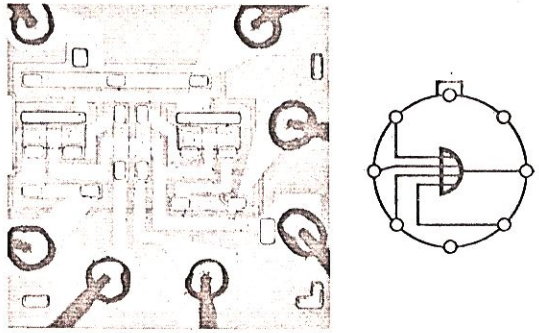
905 HALF-SHIFT REGISTER

A gated input storage element with inverter.



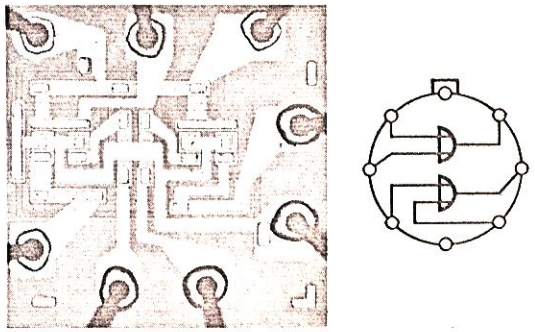
906 HALF-SHIFT REGISTER

A gated input storage element without inverter (reduces power dissipation).



907 FOUR-INPUT GATE

A four-input NAND/NOR circuit.



914 DUAL TWO-INPUT GATE

Dual NAND/NOR gates capable of forming a flip-flop, noninverting gate, or gate plus inverter.